REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 9 and 11-17 are pending in this application. No claims are amended herein. No claims are canceled herein. Claim 17 is newly added herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. § 112

Claim 15 is rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable to one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The rejection derives from absence of support within applicant's specification for the limitation of a bond wire having a minimum of one loop bonded to applicant's bond pad.

In response, applicant has amended applicant's specification at paragraph 0048 accordingly, to address the Examiner's concerns and provide proper correspondence with applicant's amended claim 15.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of applicant's claim 15 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claim Rejections - 35 U.S.C. §103

Claims 9, 11-14 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson et al. (U.S. Patent No. 6,294,401; hereinafter "Jacobson") in view of Shiga (U.S. Patent No. 5,396,101).

First, applicant notes that the Examiner at page 3, lines 10-12 of the Office communication mailed 31 December 2002 acknowledges that Jacobson does not disclose a spirally patterned conductor layer having formed within its center a microelectronic structure comprising a series of at least four electrically interconnected sub-patterns to attenuate eddy currents within the microelectronic structure (in accord with applicant's twice amended claim 9 and claim 16). Applicant also notes that the Examiner at page 3, lines 12-15 of the Office communication mailed 31 December 2003 nonetheless asserts that it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the interconnected sub-patterns of Jacobson by adding more sub-patterns to provide applicant's claimed invention since it has been held that mere duplication of essential working parts of a device involves only routine skill in the art (citing *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8).

In response, applicant understands that the Examiner is apparently employing the legal precedent of *St. Regis Paper* for purposes of providing rationale supporting the Examiner's modification of Jacobson for purposes of rejecting applicant's claims to applicant's invention under 35 U.S.C. § 103.

Applicant further notes that MPEP 2144 provides that "[i]f the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the court [for rejecting the applicant's claims to the applicant's

invention under 35 U.S.C. § 103]. Thus, MPEP 2144 apparently provides as a threshold issue a determination of factual similarity of: (1) cited legal precedent; and (2) an applicant's application, since in absence thereof cited legal precedent may apparently not be employed in rejecting an applicant's claims to the applicant's invention under 35 U.S.C. § 103.

Applicant thus respectfully requests that *St. Regis Paper* properly be made of record and a copy thereof be provided to applicant so that applicant may properly assess and challenge factual similarity thereof with applicant's disclosed and claimed invention. At present, applicant asserts that appropriate factual similarity has not been demonstrated by the Examiner (as is apparently implicitly required in accord with MPEP 2144) and thus applicant's twice amended claim 1 and claim 16 (and claims dependent thereupon) may not properly be rejected under 35 U.S.C. § 103(a) employing the cited legal precedent *St. Regis Paper,* for reasons as cited by the Examiner.

Second, applicant notes that the Examiner at page 3, last sentence of the Office communication mailed 31 December 2002 predicates suggestion or motivation to modify or combine Jacobson with Shiga (to provide applicant's invention as disclosed and claimed within twice amended claim 1 and claim 16) upon Shiga's disclosure of attenuation of eddy currents within a microelectronic device such as to provide an increase in operating frequency of the microelectronic device.

In response, applicant notes that the Examiner has accurately cited Shiga's disclosure with respect to attenuation of eddy currents and increase in operating frequency within a microelectronic device. However, with respect to Jacobson, applicant notes that Jacobson's electronic identification tag (Fig. 4 and col. 7, lines 9-30) which comprises an

inductor and a pair of interconnected capacitors is unlikely to experience eddy currents in its static state since there is no indication that Jacobson's electronic identification tag is powered in its static state. In addition applicant again notes that Jacobson's electronic identification tag's response is a digital response activated by a magnetic field from an external coil and controlled by a separate logic circuit within Jacobson's electronic identification tag. Applicant is unable to locate within Jacobson any suggestion that eddy currents would actually occur incident to external magnetic field activation of Jacobson's electronic identification tag or that additional patterning of Jacobson's pair of interconnected capacitors to effect eddy current attenuation would facilitate a desired result, such as an increased operating frequency, within Jacobson's electronic identification tag.

Thus, applicant asserts that Jacobson may not properly be combined with Shiga to reject any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a) for reasons as suggested by the Examiner, since the reasons as suggested by the Examiner appear inapplicable to Jacobson's invention. The fact that references can be combined or modified is by itself insufficient suggestion or motivation for modification or combination of the references for providing a prima facie case of obviousness under 35 U.S.C. § 103. MPEP 2143.01.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of claims 9, 11-14 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of Shiga be withdrawn.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of DiCaprio et al. (U.S. Patent No. 6,452,278; hereinafter "DiCaprio").

Applicant notes that the Examiner at page 4, lines 13-15 of the Office communication mailed 31 December 2002 predicates suggestion or motivation for modification or combination of Jacobson with DiCaprio (to provide applicant's claimed invention having a bond pad and a looped bond wire connected to the bond pad) upon DiCaprio's disclosure (col. 2, lines 48-50) of a desire to minimize a height of an electronics package.

In response, applicant asserts that there exists no suggestion or motivation for modification or combination of Jacobson with DiCaprio for reasons as cited by the Examiner insofar as Jacobson's electronic identification tag is activated by a magnetic field from an external coil and thus requires no apparent bond wire connection in a first instance, whether or not the bond wire connection minimizes the height of Jacobson's package. In addition, applicant notes that applicant's multiply looped bond wire would likely contribute to an increase in height of an electronics package rather than a decrease in height of the electronics package and thus DiCaprio teaches away from that which is disclosed and claimed by applicant. MPEP 2141.02.

Thus, since the reasons as advanced by the Examiner for combining Jacobson with DiCaprio appear inapplicable to Jacobson or applicant's invention, and since DiCaprio appears to teach away from that which is disclosed and claimed by applicant, applicant asserts that Jacobson may not properly be combined with DiCaprio for purposes of rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson in view of DiCaprio be withdrawn.

Other Considerations

Applicant has newly added claim 17 which is styled after applicant's claim 16, but which provides for a plurality of loops within applicant's bond wire bonded to applicant's bond pad rather than at least one loop within applicant's bond wire. Support for newly added claim 17 is found within applicant's specification at paragraph 0048 as amended, which further finds support within applicant's Fig. 3 as originally filed.

Applicant acknowledges the prior art of record newly cited by the Examiner but not employed in rejecting applicant's claims to applicant's invention, in particular Seefeldt et al (U.S. Patent No. 6,310,387), as generally pertinent to applicant's invention.

A fee is due as a result of this Amendment and Response. The Commissioner is hereby authorized to charge Deposit Account No. 50-0484 the required fee amount.

SUMMARY

Applicant's invention as disclosed and claimed within twice amended claim 9, amended claim 15, claim 16 and newly added claim 17 is directed towards a microelectronic fabrication, wherein the microelectronic fabrication comprises formed over a substrate a spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer forms a planar spiral inductor, and the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns

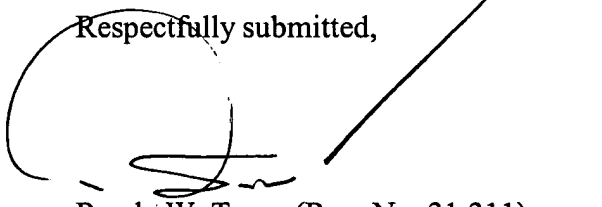
(preferably at least four) to which may be bonded a bond wire having incorporated therein a minimum of one loop (and preferably a plurality of loops), such as to attenuate eddy currents within the microelectronic structure. The prior art of record employed in rejecting applicant's claims to applicant's invention may not properly be modified or combined for purposes of rejecting applicant's claims to applicant's invention, for reasons as suggested by the Examiner.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,



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APPENDIX

PORTION OF THE SPECIFICATION

(MARKED-UP WITH CURRENT REVISIONS)

0048 Notable within the planar spiral inductor structure of the present invention as illustrated within the schematic cross-sectional diagram of Fig. 3 is that the bond wire 15 has incorporated therein additional lead length, in particular as illustrated within the context of several loops (i.e., a minimum of one loop and preferably a plurality of loops), compressed in a location near the spirally patterned conductor layer 12d which forms the bond pad 14. Within the present invention, the presence of the lead length within the bond wire 15 with the minimum of one loop and preferably the plurality of loops at the location near the spirally patterned conductor layer 12d which forms the bond pad 14 provides for an additional tunable inductance when fabricating a microelectronic inductor structure in accord with the present invention. Typically and preferably, the lead length within the bond wire is formed of a length from about 1000 to about 100000 microns, to provide a tunable inductance to the microelectronic inductor structure whose schematic cross-sectional diagram is illustrated in Fig. 3 of from about 0.5 to about 5 nano-Henry in addition to a base inductance of the planar spiral inductor structure as illustrated within the schematic plan view diagram of Fig. 1 of from about 0.5 to about 30 nano-Henry.

APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. - 8. (canceled)

9. (twice amended) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns.

10. (canceled)

11. The microelectronic fabrication of claim 9 wherein the microelectronic structure is selected from the group consisting of resistors, diodes, capacitors, bond pads and aggregates thereof.

12. The microelectronic fabrication of claim 9 wherein the microelectronic structure comprises a capacitor electrically connected with a bond pad.

13. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

14. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed in a geometric shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, an ellipse and a circle.

15. (amended) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.

16. A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a

planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns, such as to attenuate eddy currents within the microelectronic structure.

17. (newly added) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns; and

a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a plurality of loops.